In-circuit, Run-time Compiler of Finite State Machines for the UTIA EdkDSP Customizable Accelerators

Jiří Kadlec

ÚTIA AV ČR v.v.i.
Dep. of Signal Processing
Prague, Czech Republic
http://www.utia.cas.cz
kadlec@utia.cas.cz

Abstract:

We present technology enabling automation of generation, configuration and compilation of both software and hardware component for systems with CPU core and specialized UTIA EdkDSP hardware accelerators. The finite state machines (FSMs) of these accelerators can be recompiled in-circuit and in the run-time as background task. FSMs are implemented as on-fly reconfigurable 8-bit soft processors (Xilinx PicoBlaze KCPSM3) reprogrammable by change of the locally compiled firmware. Each FPGA compiles this firmware by background execution of our EdkDSP Compiler in the real-time. It is executed on the MicroBlaze CPU as process running in the background, without stopping of the application. These customizable accelerators are compatible with the PLB bus of the Xilinx MicroBlaze 8.20.b soft-core processor on the Xilinx Spartan FPGA (Xilinx ISE 13.4, EDK 13.4, SDK 13.4). Each EdkDSP FPGA also supports the Ethernet point-to point connectivity and local file system based on the nonMMU PetaLinux. TCP-IP serves for compilation and dynamic download of source code of the firmware to FPGAs. Remote control from standard WWW browser is implemented by HTTP server running on each FPGA chip. Remote user interface is integrated into the Xilinx release of the Eclipse environment forming the Xilinx SDK 13.4. It is compatible with the Win XP, Win 7 (32/64 bit), as well as Linux. The PicoBlaze KCPSM3 with fix firmware are also used to implement EdkDSP I/Os like: LCD; PWM; ADC; DAC; FREQ_CNT. These EdkDSP I/Os are extensions of the I/O developed by the UTIA team in the VLAM project co-funded by the MEYS CZ Project No. C06008, finalized in 2011. EdkDSP HW is used in Artemis project SMECY.

Academy of Sciences of the Czech Republic
Institute of Information Theory and Automation
department of signal processing

In-circuit, Run-time Compiler of Finite State Machines for the UTIA EdkDSP Customizable Accelerators

Jiří Kadlec
ÚTIA AV ČR v.v.i.
Dep. of Signal Processing
Prague, Czech Republic
http://www.utia.cas.cz
kadlec@utia.cas.cz

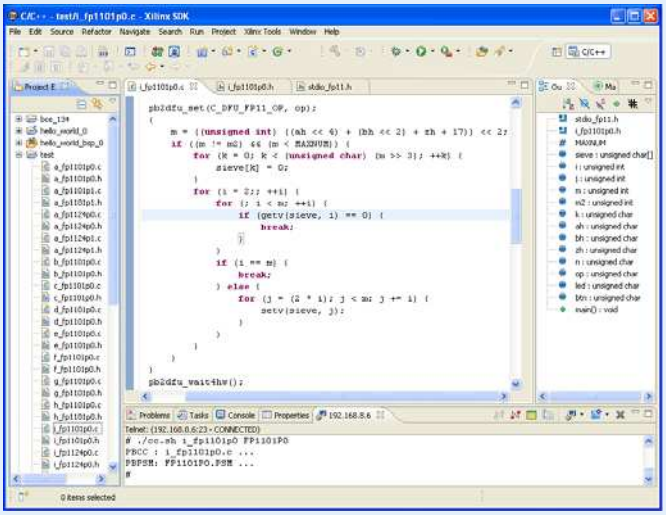
Compiler of the FSMs

- We present technology enabling automation of generation, configuration and compilation of both software and hardware component for systems with CPU core and specialized UTIA EdkDSP hardware accelerators. The finite state machines (FSMs) of these accelerators can be recompiled in-circuit and in the run-time as background task.
- FSMs are implemented as on-fly reconfigurable 8-bit soft processors (Xilinx PicoBlaze KCPSM3) reprogrammable by change of the locally compiled firmware. Each FPGA compiles this firmware by background execution of our EdkDSP Compiler in the real-time. It is executed on the MicroBlaze CPU as process running in the background, without stopping of the application).
- These customizable accelerators are compatible with the PLB bus of the Xilinx MicroBlaze 8.20.b soft-core processor on the Xilinx Spartan FPGA (Xilinx ISE 13.4, EDK 13.4, SDK 13.4).

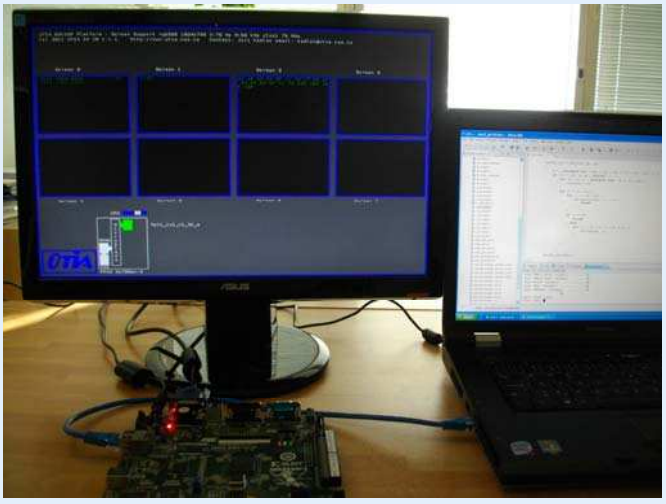
TCP-IP and EdkDSP I/Os

- Each EdkDSP FPGA also supports the Ethernet point-to point connectivity and local file system based on the nonMMU PetaLinux. TCP-IP serves for compilation and dynamic download of source code of the firmware to FPGAs. Remote control from standard WWW browser is implemented by HTTP server running on each FPGA chip.
- Remote user interface is integrated into the Xilinx release of the Eclipse environment forming the Xilinx SDK 13.4. It is compatible with the Win XP, Win 7 (32/64 bit), as well as Linux.
- The PicoBlaze KCPSM3 with fix firmware are also used to implement EdkDSP I/Os like: LCD; PWM; ADC; DAC; FREQ_CNT. These EdkDSP I/Os are extensions of the I/O developed by the UTIA team in the VLAM project co-funded by the MEYS CZ Project No. C06008, finalized in 2011.
- EdkDSP HW is used in Artemis project SMECY.

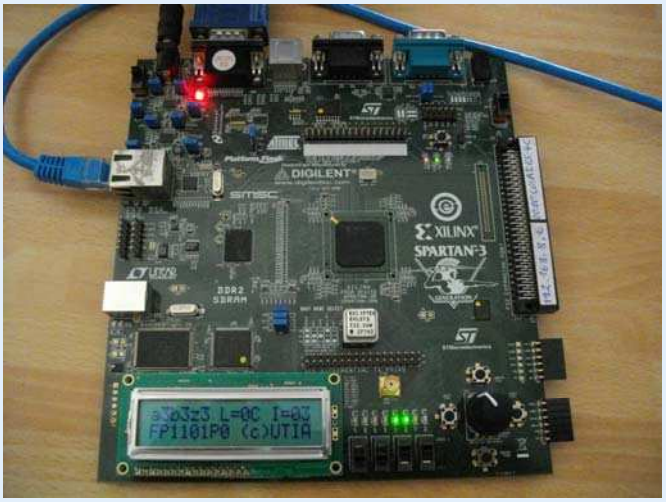
In-circuit FSM Compiler. Compile Time < 100 sec. (3s700an 50 MHz)



Local screens for print, visualization are generated by FPGAs.



Compatible with Xilinx Starter Kits: 3s500e, 3s700an, 6slx16, 6slx45t



http://sp.utia.cz

ÚTIA AV ČR, v.v.i.
Pod Vodárenskou věží 4
182 08 Praha 8
Czech Republic
tel: (+420) 26605 2216
fax: (+420) 26605 2511
email: sp@utia.cz
www: sp.utia.cz